MITEL
SEMICONDUCTOR

## SEMICONDUCTOR PRODUCT PROFILE

The high reliability and performance standards along with technology and design capabilities are key ingredients towards a leadership position in any area of the semiconductor industry. It has taken well over a year for Mitel Semiconductor to shed its position as just another good supplier of CMOS integrated circuits by developing a multiplicity of technologies and proprietary designed LSI circuits.

Our capabilities cover a broad spectrum of technologies:

| | |
|---|---|
| CMOS | Metal Gate & Silicon Gate |
| PMOS & NMOS | Metal Gate & Silicon Gate |
| ISO-CMOS | Silicon Gate |
| ISO-CCD | Double-Poly |

Mitel's proprietary products are grouped into their major functions or applications. These include:

| | |
|---|---|
| TELECOMMUNICATION CIRCUITS | CMOS/ISO CMOS |
| TRANSVERSAL FILTERS | ISO-CCD |
| MEMORIES – CMOS STATIC RAM's/MICROPROCESSORS | ISO CMOS |
| ALPHA-NUMERIC DISPLAY DRIVERS/DECODERS | CMOS |
| ANALOG SWITCHES/GATES | CMOS |
| DETECTORS/TIMERS/ALARMS | CMOS |

All products manufactured by Mitel undergo quality inspections and testing in accordance with MIL-M-38510 and MIL-STD-883, Method 5005.1. Reliability screening is in accordance to MIL-STD-883, Method 5004.1, unless specified otherwise in your purchase order.

## PRODUCT ASSURANCE

Mitel product undergo the following standard processing, tests and screens:

WAFER PROBE TEST – Every die (chip) on the wafer is 100% tested for: Electrical functionality operation. Parametric, AC & DC operation. Parametric leakage ($I_{DD}$).

ASSEMBLY – The assembly of Mitel product is processed to the exacting quality inspection and monitoring standards as specified under MIL-STD-883.

QUALITY CONTROL – Visual inspection; all product undergo 100% visual inspection per MIL-STD-883, Method 2010.2, Condition B.

STABILIZATION BAKE – Method 1008, C; 150°C, 24 Hours. This heat stresses the device to accelerate degradation failure candidates due to oxide or other process contaminents, and helps to eliminate marginal bonds and electrical connections.

TEMP. CYCLE – Method 1010C; –65°C to 150°C, 10 cycles for ceramic packages and 5 cycles for plastic packages. Exposing the product to a 215°C temperature change stresses the chip, wire bonds and package. The extreme temperature variation repeated many times places all parts of the product into a continuous stress mode, and helps accelerate catastrophic failure candidates.

QUALITY ASSURANCE – All product, prior to shipment, undergo the following QA Acceptance tests: Functional: 25°C, AQL; 0.28% Plastic – 25°C, AQL; 0.2% Ceramic / DC: 25°C, AQL 0.65% / DC: Temp's AQL 2.2% / AC: 25°C, AQL 1.0%.

In addition to the above standard processes, the following optional screens offer added levels of assurance and reliability to the product:

FINE LEAK – Method 1014, B (Tracer-Flo) checks the hermeticity of the ceramic package between 1 x 10-5 and 1 x 10-8 atmcc/sec. leak rates.

GROSS LEAK – Method 1014, C checks the package hermeticity up to 1 x 10-5 atmcc/sec.

BURN-IN – Method 1015, 125°C for 168 Hours or 150°C for 48 Hours (accelerated).

Continual quality and reliability evaluations are conducted on Mitel products, both in-house and by independent test laboratories. All products undergo periodic quality conformance inspection and testing in accordance with MIL-STD-883, Method 5005.1. Plastic packaged devices undergo added temperature cycling and temperature-humidity (85/85) tests designed to assure the package and product integrity.

MITEL
Technical Data

# MT8804B

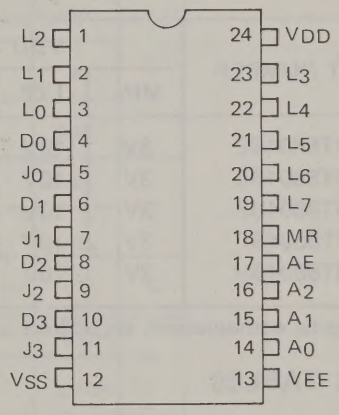
## CMOS/LSI 8 x 4 ANALOG SWITCH ARRAY

## DESCRIPTION

The 8804B is a CMOS/LSI 8 x 4 Analog Switch Array incorporating control memory (32-bits), decoder and digital logic-level convertors. This circuit has digitally controlled analog switches having very low "ON" impedance and very low "OFF" leakage current. Switches will operate with analog signals at frequencies to 40 MHz and up to 18V p-p. A "HIGH" on the Master Reset input switches all channels "OFF" and clears the memory. This device is ideal for crosspoint switching applications. See page 2 for Part Numbers.

- CMOS POWER CONSUMPTION (1μW typ.)
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS: To 18V, ± 9V peak
- LOW "ON" RESISTANCE: 50Ω (TYP.)
- MATCHED SWITCH CHARACTERISTICS: 5Ω (TYP.) BETWEEN RON VALUES
- HIGH "ON/OFF" OUTPUT VOLTAGE RATIO: 65 dB (TYP.) at fis = 10KHz, RL = 10KΩ
- HIGH DEGREE OF LINEARITY: <0.5% DISTORTION AT fis = 1KHz, Vis = 5Vp-p, VDD − VSS ≥ 10V, RL = 10KΩ
- LOW CROSSTALK BETWEEN SWITCHES: −50dB at fis = 0.9 MHz, RL = 1KΩ
- TRANSMITS FREQUENCIES UP TO 40 MHz
- ASYNCHRONOUS MEMORY OPERATION:
- ADDRESS DECODING ON CHIP
- MASTER RESET OF CONTROL MEMORY
- STD. 24-PIN PACKAGES

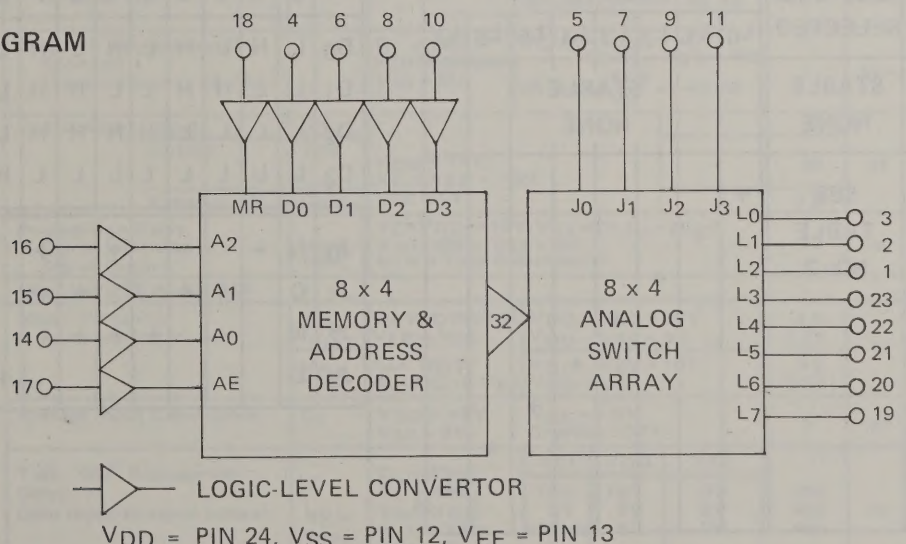
## CONNECTION DIAGRAM (TOP VIEW)




## PIN NAMES

| | |
|---|---|
| $A_0$, $A_1$, $A_2$ | Address (Active HIGH) Inputs |
| AE | Address Enable (Active HIGH) Input |
| MR | Memory Reset (Active HIGH) Input |
| $D_0$, $D_1$, $D_2$, $D_3$ | Data (Active HIGH) Inputs |
| $J_0$, $J_1$, $J_2$, $J_3$ | Junctor (Analog Swx) Inputs |
| $L_0$, $L_1$, $L_2$, $L_3$, $L_4$, $L_5$, $L_6$, $L_7$ | Line (Analog Swx) Outputs |

## BLOCK DIAGRAM




$V_{DD}$ = PIN 24, $V_{SS}$ = PIN 12, $V_{EE}$ = PIN 13

MITEL SEMICONDUCTOR, 18 Airport Blvd., Bromont, Quebec, Canada J0E 1L0, (514) 534-2321 Telex: 05-267474
MITEL SEMICONDUCTOR, P.O. Box 13089 Kanata, Ottawa, Ontario, Canada K2K 1X3, (613) 592-2122 Telex: 05-34596
MITEL SEMICONDUCTOR, 1745 Jefferson Davis Hwy., Suite 611, Arlington, Va, 22202, (703) 243-1600
MITEL SEMICONDUCTOR, St. Lawrence Industrial Park, P.O. Box 207, Ogdensburg, N.Y., U.S.A., 13669, (315) 393-1212 Twx: 510-259-4071
MITEL SEMICONDUCTOR, 2831 Camino Del Rio South, Suite 310, San Diego, Calif. 92108, (714) 299-4888
MITEL SEMICONDUCTOR, 1A Albert Street, Slough, England, Tel.: 28154 Telex: 51-847730
MITEL SEMICONDUCTOR, Park-In Commercial Centre, Suite 1423, 56 Dundas Street, Mongkok, Kowloon, Hong Kong, Tlx: 802-84931
MITEL SEMICONDUCTOR, P.O. Box 10, Tahoma Calif. 95733, (916) 525-5154

## FUNCTIONAL DESCRIPTION

The 8804B is a CMOS/LSI 8 x 4 Analog Switch Array designed so that the analog switches can be connected such that the four input junctors may be connected to any combination of the eight output lines depending on what code is stored in the 32-bit memory.

The memory is organized in eight 4-bit words. The logic level signals applied to the four data inputs are transferred to the selected memory locations by the code on the three address inputs whenever a logic HIGH is applied to the address enable input (AE). A logic HIGH set in memory location will cause the corresponding analog switch location to be "ON". A HIGH on the memory reset input (MR) will cause all locations to be in a LOW state and all analog switches to be "OFF".

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage at any pin | $V_{SS}$ −0.3V to 18.5V |
| Storage temperature | −65°C to 150°C |
| Operating temperature | −40°C to 85°C and |
| | −55°C to 125°C |

$V_{DD} - V_{EE} = 18.5V$, $V_{DD} - V_{SS} = 18.5V$

## GUARANTEED OPERATING RANGES

| PART NUMBER | VDD | | | VEE* | | | TEMPERATURE | PACKAGE |
|---|---|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | |
| MT8804BE | 3V | 10V | 18V | 0V | −5V | −15V | −40°C to 85°C | 24 Pin Epoxy DIP |
| MT8804BC | 3V | 10V | 18V | 0V | −5V | −15V | −40°C to 85°C | 24 Pin Ceramic DIP |
| MT8804BF | 3V | 10V | 18V | 0V | −5V | −15V | −55°C to 125°C | 24 Pin Ceramic DIP |
| MT8804BI | 3V | 10V | 18V | 0V | −5V | −15V | −55°C to 125°C | 24 Pad Tested Chip |
| MT8804BH | 3V | 10V | 18V | 0V | −5V | −15V | −40°C to 85°C | 24 Pad Tested Chip |

* All digital combinations on address and data inputs; all analog inputs: $V_{EE} \leq V_I \leq V_{DD}$

## LOGIC TABLES

TABLE NO. 1 – ANALOG SWX. SELECTED

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDRESS | | | | MEM. RESET | JUNCTOR(S) SELECTED | LINE SELECTED | | | | | | | |
| $A_0$ | $A_1$ | $A_2$ | $A_E$ | | | $L_0$ | $L_1$ | $L_2$ | $L_3$ | $L_4$ | $L_5$ | $L_6$ | $L_7$ |
| X | X | X | L | L | STABLE | STABLE | | | | | | | |
| X | X | X | X | H | NONE | NONE | | | | | | | |
| L | L | L | H | L | SEE TABLE NO. 2 | + | | | | | | | |
| H | L | L | H | L | | | + | | | | | | |
| L | H | L | H | L | | | | + | | | | | |
| H | H | L | H | L | | | | | + | | | | |
| L | L | H | H | L | | | | | | + | | | |
| H | L | H | H | L | | | | | | | + | | |
| L | H | H | H | L | | | | | | | | + | |
| H | H | H | H | L | | | | | | | | | + |

TABLE NO. 2 – JUNCTOR(S) SELECTED

| DATA INPUT CODE | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| $D_0$ | L | H | L | H | L | H | L | H | L | H | L | H | L | H | L | H |
| $D_1$ | L | L | H | H | L | L | H | H | L | L | H | H | L | L | H | H |
| $D_2$ | L | L | L | L | H | H | H | H | L | L | L | L | H | H | H | H |
| $D_3$ | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H |
| $J_0$ | N | + | | + | | + | | + | | + | | + | | + | | + |
| $J_1$ | O | | + | + | | | + | + | | | + | + | | | + | + |
| $J_2$ | N | | | | + | + | + | + | | | | | + | + | + | + |
| $J_3$ | E | | | | | | | | + | + | + | + | + | + | + | + |

WHERE:

X = Don't care condition
+ = Selected switch(es)
L = LOW logic state
H = HIGH logic state

## ELECTRICAL CHARACTERISTICS at $T_A$ = 25°C

| CHARACTERISTIC | SYMBOL | TEST CONDITIONS | | | TYPICAL VALUES | UNITS |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ | $V_{SS}$ | $V_{EE}$ | | |
| Quiescent Device Current | $I_L$ | +10V | 0V | 0V | 0.1 | µA |
| | | OR | | | | |
| | | +5V | 0V | −5V | | |
| | | | NOTE 1 | | | |
| Quiescent Device Dissipation per Package | $P_D$ | +10V | 0V | 0V | 1 | µW |
| | | OR | | | | |
| | | +5V | 0V | −5V | | |
| | | | NOTE 1 | | | |

NOTE 1: All digital combinations on address inputs; all analog inputs

$V_{EE} \leq V_I \leq V_{DD}$

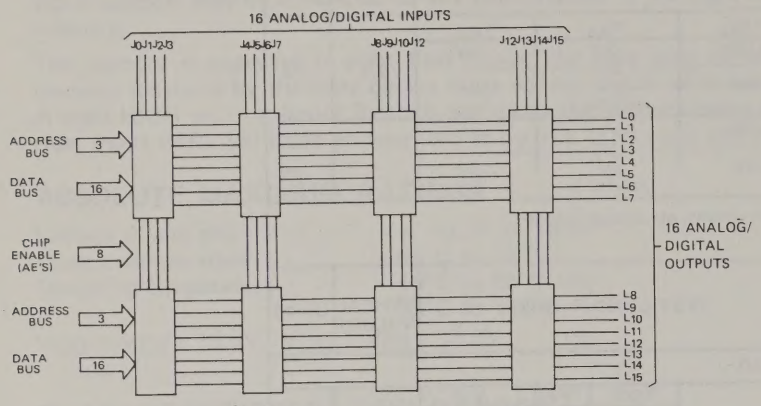
| CHARACTERISTIC | SYMBOL | TEST CONDITIONS | | | | TYPICAL VALUES | UNITS |
|---|---|---|---|---|---|---|---|
| SIGNAL INPUTS (Vis) AND OUTPUTS (Vos) | | | | | | | |
| | | | $V_{DD}$ | $V_{EE}$ | $V_{IS}$ | | |
| "ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$) | $R_{ON}$ | $R_L$ = 10kΩ, $V_{SS}$ = 0 | +9V OR +18V | −9V 0V | – | 50 | Ω |
| | | | +5V OR +10V | −5V 0V | – | 90 | |
| | | | +2.5V OR +5V | −2.5V 0V | – | 200 | |
| Δ"ON" Resistance Between Any 2 Channels | $\Delta R_{ON}$ | (Any channel selected) | +9V OR +18V | −9V 0V | – | 5 | Ω |
| | | | +5V OR +10V | −5V 0V | – | 10 | |
| Sine Wave Response (Distortion) | | $R_L$ = 10kΩ, $V_{SS}$ = 0, $f_{is}$ = 1kHz | +9V<br>+5V<br>+2.5V | −9V<br>−5V<br>−2.5V | 5V (p-p)▲ | 0.1<br>0.2<br>1 | % |
| OFF Channel Leakage Current: Any Channel "OFF" | | $V_{SS}$ = 0V | +5V | (= $V_C$) −5V | – | ±0.01 | nA |
| All Channels "OFF" | | $V_{SS}$ = 0V | +5V | (= $V_C$) −5V | | ±0.04 | |
| Frequency Response— Channel "ON" (Sine Wave Input) | | $R_L$ = 1kΩ, $V_{is}$ = 5V (p-p), $V_{SS}$ = 0V | $V_C = V_{DD}$=+5V, $V_{EE}$=5V; $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -3$ dB | | | 40 | MHz |
| Feedthrough Channel "OFF" | | | $V_{DD}$=+5V, $V_C$=$V_{EE}$=−5V; $20 \log_{10} \frac{V_{DS}}{V_{is}} = -40$ dB | | | 1 | MHz |
| Crosstalk Between any 2 Channels (Frequency at − 40 dB) | | $R_L$ = 1kΩ, $V_{is}$(A) = 5V (p-p), $V_{SS}$ = 0V | $V_C$(A) = $V_{DD}$ = +5V, $V_C$(D) = $V_{EE}$=−5V; $20 \log_{10} \frac{V_{OS}}{V_{is}} = -40$ dB | | | 1 | MHz |
| Capacitance: Input | $C_{IS}$ | $V_{DD}$ = +5V, $V_C$ = $V_{EE}$ = −5V, $V_{SS}$ = 0V | | | | 5 | pF |
| Output | $C_{OS}$ | | | | | 20 | |
| Feedthrough | $C_{IOS}$ | | | | | 0.2 | |
| Propagation Delay Signal Input-to-Signal Output | $t_{PLH}$ $t_{PHL}$ | $V_C$=$V_{DD}$=+10V, $V_{EE}$=0V, $C_L$=50 pF, $V_{is}$ = 10V•, $V_{SS}$ = 0V, $t_r$, $t_f$ = 20ns (input signal) | | | | 10 | ns |
| (VC) INPUTS $A_i$ AND $D_j$ | | | | | | | |
| Noise Immunity (Any control input) | $V_{NL}$ | $V_{is}$=$V_{DD}$ thru 1kΩ, $V_{EE}$ = $V_{SS}$ | $V_{DD} - V_{SS}$ = 10V<br>$V_{DD} - V_{SS}$ = 5V | | | 4.5<br>2.25 | V |
| | $V_{NH}$ | $I_{is}$ = 10µA, $R_L$=1kΩ to $V_{EE}$ | $V_{DD} - V_{SS}$ = 10V<br>$V_{DD} - V_{SS}$ = 5V | | | 4.5<br>2.25 | |
| Average Input Capacitance | $C_I$ | $V_{DD}$ = +5V, $V_{SS}$ = 0V | $V_{EE}$ = −5V, Channel "OFF" | | | 5 | pF |
| | | | $V_C$• | $V_{DD}$ | $V_{EE}$ | | |
| Turn "ON" Propagation Delay: • Data Input-to-signal output | $t_{PLH}$ $t_{PHL}$ | $C_L$ = 50pF, $R_L$ = 10kΩ, $V_{is} \leq V_{DD}$, $t_r$, $t_f$ = 20ns, $V_{SS}$ = 0V | 10V<br>5V<br>+5V to −5V | 10V<br>5V<br>5V | 0V<br>0V<br>−5V | 200<br>400<br>400 | ns |
| Address Enable to-Signal Output | | $C_L$ = 50pF, $R_L$ = 10kΩ, $V_{is}$ = $V_{DD}$, $t_r$, $t_f$ = 20ns | 10V<br>5V | 10V<br>5V | 0V<br>0V | 300<br>600 | ns |
| Memory Reset Recovery Time• | – | $V_{DD}$ = 10V | | | | 200 | ns |

• Time after reset is removed during which channel information is invalid / • Square wave / ▲ Symmetrical about 0 volts.

• Channel Overlap = Turn-on propagation delay, where channel overlap is delined as the duration after control signal change during which two channels may be on together.

## APPLICATIONS

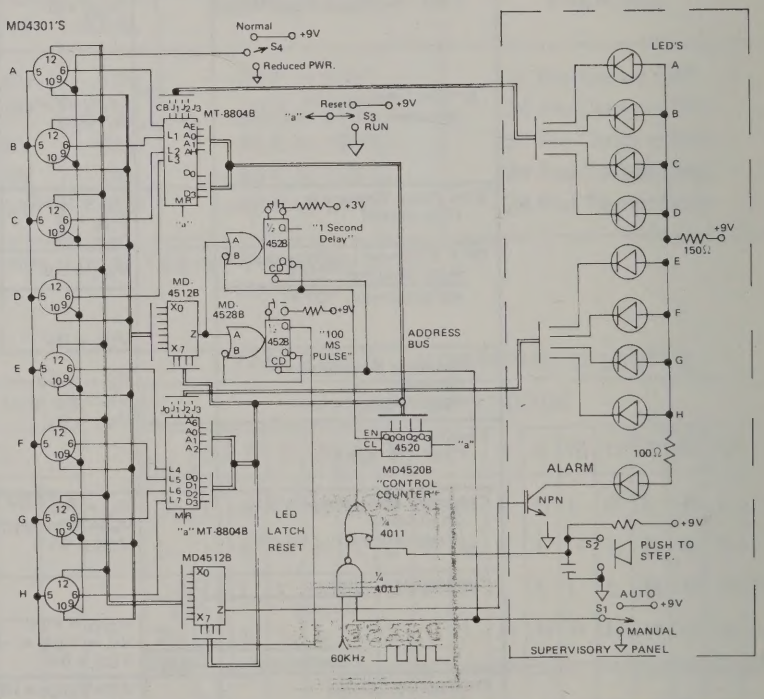
### 16-INPUT ANALOG MIXER/MULTIPLEXER CIRCUIT




256 switching combinations can be realized using eight MT8804B CMOS/LSI 8 x 4 Analog Switch Arrays. Each of the 16 inputs can be connected to any of the 16 outputs simultaneously. The address input will select the output line, while the data input will select the junctor input or combination of inputs to be switched onto the selected output line.

### MULTIPLE-DETECTOR/ALARM SYSTEM WITH REMOTE AUTOMATIC SUPERVISORY DISPLAY AND CONTROL PANEL.

The address control counter (MD4520B) causes the eight detector (MD4301A's) locations to be scanned once every 267 µS. If any detector is activated in any way, the counter will immediately stop at that location. The situation can be quickly analysed using the supervisory panel as follows:




| PANEL INDICATION* | | | INDICATED CONDITION |
|---|---|---|---|
| HORN | ALARM LIGHT | LED'S | |
| No Sound | OFF | Pulsing | Normal — Standby |
| ON | ON | ON | Continuously Activated Detector (s). |
| Pulsed | Pulsed | Pulsing | Momentarily Activated Detector (s). |
| Pulsing | OFF | Pulsing | Low Battery Voltage at Location (s). |

*$S_1$ = Auto; $S_2$ = OFF; $S_3$ = RUN; $S_4$ = Don't Care

May 1978

MITEL

Mitel Incorporated, National Headquarters: 1745 Jefferson Davis Highway, Suite 603,
Arlington, Virginia, USA 22202 Telephone: (703) 243-1600, TWX 710 955 0026

# MITEL SEMICONDUCTOR PRICE GUIDE

| PART NUMBER | DESCRIPTION | 1-24 | 24-99 | 100 | 1000 | 10,000 |
|---|---|---|---|---|---|---|
| MH88200 | DTMF RECEIVER | 98.00 | 98.00 | 90.00 | 79.00 | 75.00 |
| MT8820AN | DTMF DECODER | 37.50 | 31.25 | 25.00 | 17.60 | 15.00 |
| MT8820AJ | | 41.25 | 34.40 | 27.50 | 19.40 | 16.50 |
| MT8804BN | 8 X 4 M U X | 10.75 | 8.95 | 7.15 | 6.30 | 5.50 |
| MT8804BJ | | 12.90 | 10.75 | 8.60 | 7.80 | 7.00 |
| ML8204AE | TONE RINGER | 2.40 | 2.00 | 1.60 | 1.36 | 1.25 |
| ML8204AE-1 | | 2.25 | 1.89 | 1.50 | 1.35 | 1.15 |
| MD4301/03AC | TIMER | 3.15 | 2.65 | 2.10 | 1.80 | 1.50 |
| MD4302/04AE | | 2.25 | 1.89 | 1.50 | 1.30 | 1.10 |
| MD4302/04AE-1 | | 2.25 | 1.89 | 1.50 | 1.35 | 1.15 |
| MD4330/31BS | LCD DRIVER | 4.20 | 3.50 | 2.80 | 2.55 | 2.30 |
| MD4330/31BM | | 8.25 | 6.90 | 5.50 | 5.00 | 4.50 |
| MD4332BS | | 4.35 | 3.65 | 2.90 | 2.65 | 2.40 |
| MD4311/4511BE | DISPLAY DRIVER | 2.10 | 1.75 | 1.40 | .80 | .70 |
| MD4368BE | | 2.20 | 1.82 | 1.45 | .85 | .75 |
| MD4368BC | | 2.95 | 2.45 | 1.95 | 1.15 | .95 |
| SIL1902AE | 1K RAM | 15.00 | 12.50 | 10.00 | 7.80 | 5.50 |
| SIL1902AC | | 16.20 | 13.50 | 10.80 | 8.40 | 5.90 |
| MD4508BN | DECODER LATCH | 3.70 | 3.07 | 2.45 | 1.25 | 1.15 |
| MD4514/15BN | | 3.70 | 3.07 | 2.45 | 1.25 | 1.15 |
| MD4528BE | | 1.50 | 1.25 | 1.00 | .60 | .58 |
| MD4046BE | PHASE LOCK LP | 2.10 | 1.75 | 1.40 | .80 | .70 |
| MD4046BC | | 2.80 | 2.35 | 1.85 | 1.10 | .90 |

The package, temperature range and supply voltage range for each follows:

| PREFIX | | SUFFIX |
|---|---|---|
| MA/ML | - Linear | A.- Non-standard Parameters |
| MD | - Digital | |
| MT | - Telecom | B.- Generally, Std. JEDEC-B Spec. Parameters (3-18V) |
| MH | - Hybrid | |
| SIL | - Siltek | |

E.G.

| PREFIX | DEVICE | SUFFIX |
|---|---|---|
| MT | 8804 | BJ/B |

3V-18V operation
Package, Temperature
*MIL Process Option

*MIL-STD-883,5004.1, 125°C/168 Hr or 150°C/48 Hrs. Burn-in.

PACKAGE STYLE, TEMPERATURE RANGE

C-Ceramic DIP, 8-18 pins,-40°C to 85°C
E-Plastic DIP, 8-18 pins,-40°C to 85°C
J-Ceramic DIP, 24 pins, -40°C to 85°C
M-Ceramic DIP, 40 pins, -40°C to 85°C
N-Plastic DIP, 24 pins, -40°C to 85°C
S-Plastic DIP, 40 pins, -40°C to 85°C

MINIMUM ACCEPTABLE ORDER IS $100.

## DETECTORS – TIMERS – ALARMS:

| | | |
|---|---|---|
| CMOS/ LSI | Detector/Timer<br>Without protected MOSFET Input –<br>With protected MOSFET Input – | MD4301A<br>MD4301B |

## DISPLAY DRIVERS – DECODERS:

| | | |
|---|---|---|
| CMOS/MSI | 7-Segment Hexadecimal Decoder/Driver/Latch | MD4368A<br>MD4368B |
| | 7-Segment Hexadecimal Decoder/Driver/Latch | MD4311A<br>MD4311B |
| | 7-Segment BCD Decoder/ Driver/Latch | MD4511A<br>MD4511B |
| CMOS/ LSI | 30-Bit LCD Driver/Register | MD4330B |
| CMOS/MSI | 7-Segment LCD Decoder/Driver | MD4055B |
| CMOS/MSI | 7-Segment LCD Decoder/Driver Latch | MD4056B |

## SHIFT REGISTERS – COUNTERS:

| | | |
|---|---|---|
| CMOS/MSI | 4-Bit Parallel In/Out | SIL4035B |
| CMOS/MSI | Dual 4-Bit Serial In/Parallel Out | SIL4015B |
| CMOS/MSI | 8-Bit Sync. Parallel In/Serial Out | SIL4014B |
| CMOS/MSI | 8-Bit Assync. Parallel In/Serial Out | SIL4021B |
| CMOS/MSI | 12-Stage Binary Counter | SIL4040B |
| CMOS/MSI | 14-Stage Binary Counter | SIL4020B |
| CMOS/MSI | 14-Stage Binary Counter with Osc. | SIL4060B |
| CMOS/MSI | Dual BCD Counter (sync.) | SIL4518B |
| CMOS/MSI | Dual Binary Counter (sync.) | SIL4520B |
| CMOS/MSI | Decode Counter/Divider | SIL4017B |
| CMOS/MSI | Divide-by-8 Counter/Divider | SIL4022B |
| CMOS/MSI | Presettable Divide-by-N Counter | SIL4018B |
| CMOS/MSI | Presettable BCD/Binary – UP/DN Counter | SIL4029B |
| CMOS/MSI | Presettable BCD/ UP/DN Counter | SIL4510B |
| CMOS/MSI | Presettable Binary UP/DN Counter | SIL4516B |

## ANALOG SWITCHES – MULTIPLEXERS:

| | | |
|---|---|---|
| CMOS/ LSI | 8 x 4 Analog Switch Array With Memory | MT8804A |
| CMOS/ LSI | 8 x 4 Analog Switch Array With Memory | MT8804B |
| CMOS/MSI | Quad Bilateral Analog Switch – | SIL4016B |
| CMOS/MSI | Quad Bilateral Analog Switch – | SIL4066B |
| CMOS/MSI | 8-Channel Analog Multiplexer – | SIL4051B |
| CMOS/MSI | 4-Channel Differential Analog Multiplexer | SIL4052B |
| CMOS/MSI | Triple 2-Channel Analog Multiplexer – | SIL4053B |
| CMOS/MSI | 8-Channel Data Selector – | SIL4512B |

## DECODERS – LATCHES:

| | | |
|---|---|---|
| CMOS/ LSI | Dual 4-Bit Latch | MD4508B |
| CMOS/ LSI | 4-Bit Latch/4 to 16 Decoder | MD4514B |
| CMOS/ LSI | 4-Bit Latch/4 to 16 Decoder | MD4515B |
| CMOS/MSI | Quad Clocked "D" Latch – | SIL4042B |
| CMOS/MSI | Quad NOR R/S Latch – | SIL4043B |
| CMOS/MSI | Quad NAND R/S Latch – | SIL4044B |
| CMOS/MSI | Quad 3-State "D" Latch – | SIL4076B |

## ISO-CMOS TECHNOLOGY

MOS has grown into its present market size by virtue of its economic advantages over other forms (technologies) for circuit design. This cost advantage can ultimately be traced back to the silicon area used to implement a circuit. Since MOS devices are mostly surface devices, the smallest size can be related directly to the number of transistors, the size of each transistor, and the area required to isolate transistors from each other. Silicon-Gate MOS because of its self-aligning gate-source-drain processing characteristic, has become a standard for the MOS/LSI world. Silicon-Gate also provides an additional layer of interconnect using the poly-silicon gate material.

CMOS (complementary MOS) processing found a home in the MOS market by virtue of two unique features not available in single channel (PMOS & NMOS) processing. One being its ability to operate at very low supply voltages (under 3 volts), since the logic levels on chip are the full supply rails. Secondly, CMOS logic dissipates no power in the quiescent state and the only power used is when switching from one state to another. CMOS processing has not made many inroads into the MOS/LSI marketplace to-date mainly because of the silicon area required to isolate one transistor from another was prohibitively large.

Mitel Semiconductor has combined mature processing steps used throughout the industry to make CMOS circuits at the same (or smaller) density as single channel MOS processing. The process topology is shown in Figure 1, and is named "ISO-CMOS". This process offers all the advantages of CMOS at an area per function of PMOS or NMOS processing and is completely self-aligning throughout the process. With the reduction of area another advantage of the process becomes apparent. Switching speed in this process approaches that of TTSL Bipolar processes.

## TOPOLOGY – ISO-CMOS

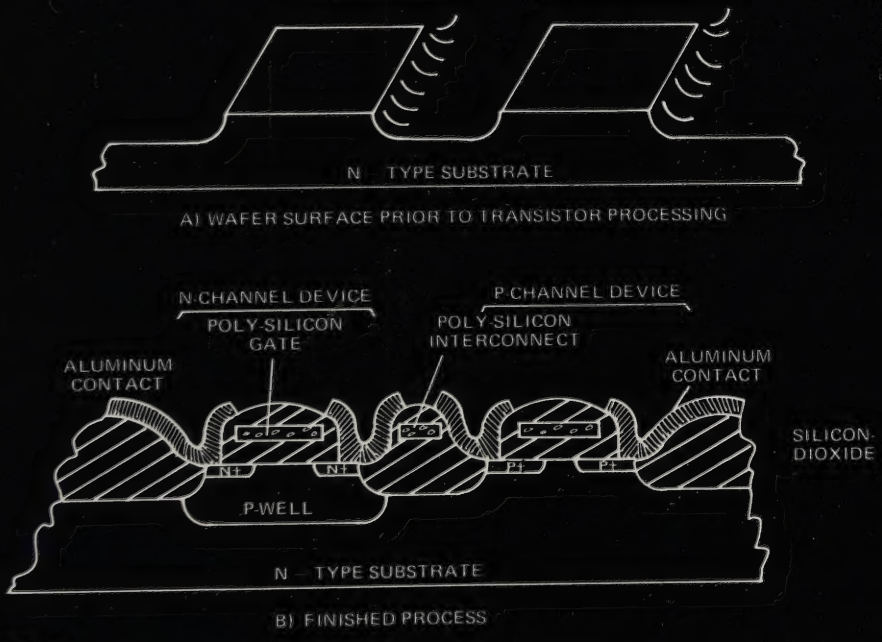
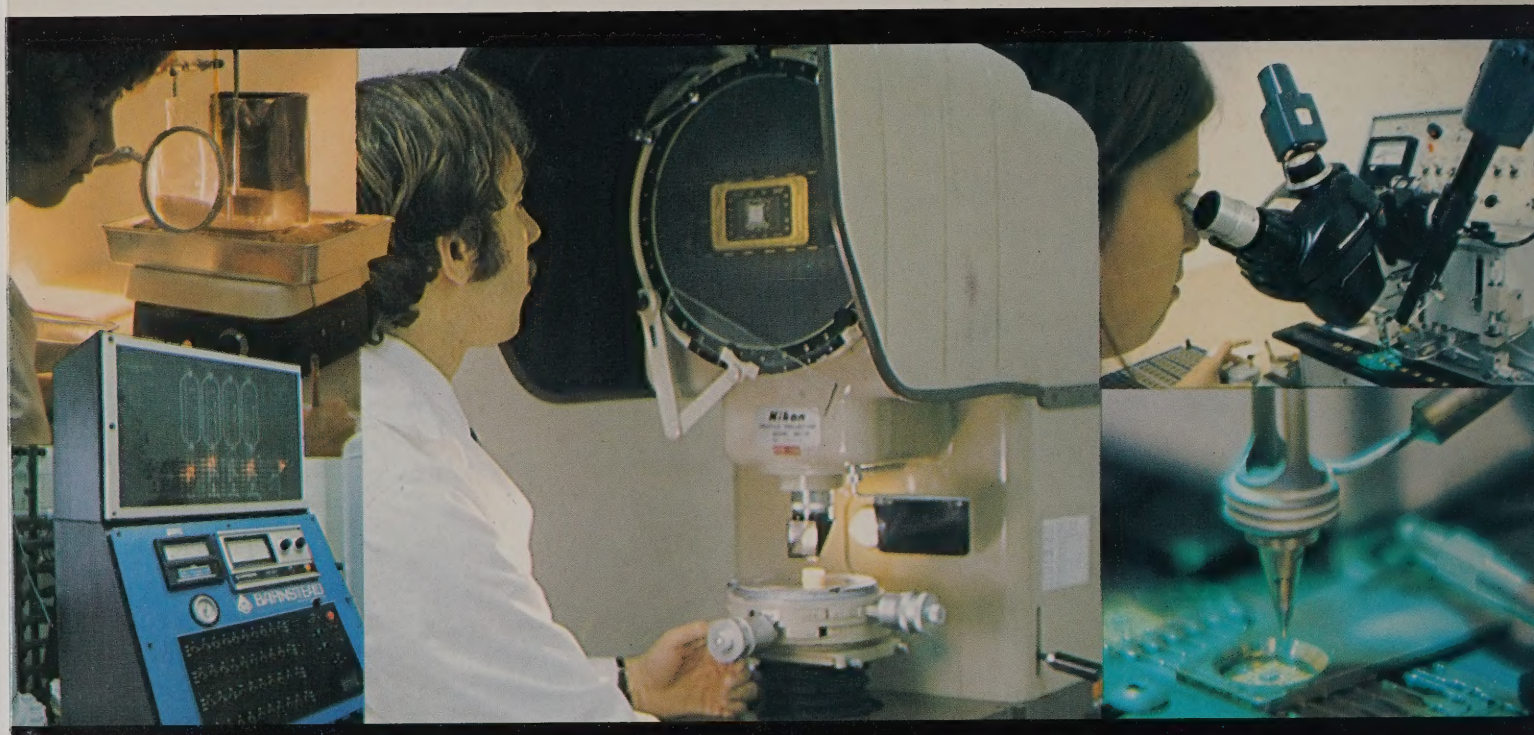



FIGURE 1.



MITEL SEMICONDUCTOR, 18 Airport Blvd., Bromont, Quebec, Canada J0E 1L0, (514)534-2321 Telex: 05-267474
MITEL SEMICONDUCTOR, P.O. Box 13089, Kanata, Ontario, Canada K2K 1X3, (613)592-2122 Telex: 05-34596
MITEL SEMICONDUCTOR, 1745 Jefferson Davis Hwy., Suite 611, Arlington, Va 22202, (703)243-1600 Twx: 710-955-0026
MITEL SEMICONDUCTOR, St. Lawrence Industrial Park, P.O. Box 207, Ogdensburg, N.Y. 13669, (315)393-1212, Twx: 910-259-4071
MITEL SEMICONDUCTOR, 7995 East Hempton Ave., Denver, Co. 80231, (303)750-8177, Twx: 910-320-2273
MITEL SEMICONDUCTOR, 1 So. Main street, Janesville, Wisc. 53545, (608)752-3537
MITEL SEMICONDUCTOR, 2831 Camino Del Rio South, Suite 310, San Diego, Ca. 92108, (714)299-4888
MITEL SEMICONDUCTOR, P.O. Box 10, Tahoma, Ca. 95733, (916)525-5154
MITEL SEMICONDUCTOR, P.O. Box 38, Katano, 00632, Puerto Rico
MITEL SEMICONDUCTOR, 1A Albert street, Slough, England, 0753-28154, Telex: 51-847730
MITEL SEMICONDUCTOR, Block 4A/D, Shannon Industrial Estate, Shannon, Ireland, 061-61433, Telex: 500-32208
MITEL SEMICONDUCTOR, Park-In Commercial Centre, Suite 1423, 56 Dundas street, Mongkok, Kowloon, Hong Kong, Telex: 802-84931